Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A resistive structure integrated in a semiconductor substrate, comprising: a ~~trench~~ plurality of successive trenches of different widths formed in the substrate and lined with dielectric material to form a single dielectric trench; and a polysilicon region, at least a portion of which is doped, the polysilicon region ~~completely~~ surrounded by the dielectric trench so that the resistive structure is isolated electrically from other components jointly integrated in the semiconductor substrate, and wherein portions of the dielectric trench are formed with ~~a~~ the plurality of trenches ~~distributed about the polysilicon region~~ to form a single dielectric region having a width that increases along the resistive structure in which a voltage drop increases.

2. (Original) The resistive structure of claim 1 wherein said polysilicon region and said dielectric region have a serpentine pattern, thereby reducing the space requirements of the resistive structure for a given resistance value.

3. (Original) The resistive structure of claim 2 wherein said serpentine pattern is formed to include rungs, said rungs are physically connected in parallel together by a metallization.

4. (Withdrawn) The resistive structure of claim 1 wherein said polysilicon region is masked and then etched to create a T-shaped structure providing connection paths of polysilicon.

5. (Currently Amended) The resistive structure of claim 1 wherein said polysilicon region comprises ~~fill~~ polysilicon that has been enhanced by implantation in ~~its~~ a surface region only of the polysilicon.

6. (Original) The resistive structure of claim 1, wherein said polysilicon region comprises two deposited layers of polysilicon, only a first of said layers being enhanced by implantation to lower the values of parasitic capacitances associated with the resistive structure.

7. (Currently Amended) The resistive structure of claim ~~1~~ 6, wherein said first polysilicon layer is enhanced by angled implantation and has a thickness dimension conforming to the sidewalls of the dielectric region ~~to prevent said region from becoming filled completely~~.

8. (Withdrawn) The resistive structure of claim 1, wherein said semiconductor substrate is a SOI substrate and comprises a plurality of dielectric trenches between wells of integrated devices therein, and that doped polysilicon intended to form the resistive structure is introduced into said trenches, the resistive structure itself requiring no additional integration area.

9. (Currently Amended) An integrated resistive structure, comprising:

at least one trench having a width that increases along a length thereof and formed in a semiconductor substrate from a plurality of successive trenches of different widths to have a depth greater than a depletion region;

a dielectric layer formed of a dielectric oxide entirely coating all walls, including a bottom wall, of the at least one trench, the dielectric layer having a width that increases along a length of the at least one trench to form a fill trench of constant width; and

a polysilicon region filling the ~~at least one~~ fill trench to be isolated dielectrically from the semiconductor substrate, the polysilicon region having at least a portion that is doped.

10. (Original) The structure of claim 12 wherein the dielectric layer has vertical and horizontal dimensions that are greater than vertical and horizontal dimensions of the polysilicon region.

11. (Canceled)

12. (Original) The structure of claim 9 wherein the polysilicon region includes a doped surface region.

13. (Original) The structure of claim 9 wherein the polysilicon region comprises first and second layers of polysilicon, the second layer being undoped and the first layer implanted with a dopant.

14. (Currently Amended) The structure of claim 13 wherein the first layer of polysilicon is implanted by angled implantation and has a thickness dimension conforming to the walls of the dielectric-coated at least one trench ~~to prevent complete filling of the at least one trench~~.

15. (Original) The substrate of claim 9, comprising a plurality of trenches coupled together electrically by metallization.

16.-26. (Canceled)

27. (Currently Amended) An integrated resistive structure, comprising:

~~at least one~~ a trench formed in a semiconductor substrate from a plurality of contiguous trenches of different widths;

a dielectric layer entirely coating all walls of the ~~at least one~~ trench, the dielectric layer having a width that increases along a length of the trench to form a fill trench; and

a polysilicon region comprising first and second layers of polysilicon filling the ~~at least one~~ fill trench, the second layer being undoped and the first layer implanted with a dopant.

28. (Currently Amended) The structure of claim 27 wherein the first layer of polysilicon is implanted by angled implantation and has a thickness dimension conforming to the walls of the dielectric-coated at least one trench ~~to prevent complete filling of the at least one trench~~.

29. (New) The structure of claim 27 wherein the polysilicon region has a constant width along a length thereof.